

MULTIMEDIA



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STUDENT ID NO

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MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2017/2018

ECP2216 – MICROCONTROLLER AND MICROPROCESSOR SYSTEMS

(All sections / Groups)

16 OCTOBER 2017
2.30 p.m – 4.30 p.m
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 13 pages with 5 Questions only.
2. Attempt **ALL FIVE COMPULSORY** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1

- (a) State any **TWO** perspectives which differentiate microcontrollers and microprocessors.

[2 marks]

- (b) Consider a 12-bit binary number, $Z = 1001\ 1010\ 1001_2$. Convert Z into decimal number, if it is

(i) an unsigned number.

[2 marks]

(ii) a signed number in two's complement format.

[3 marks]

(You are required to show out all working steps)

- (c) A 16-bit microcontroller is designed to access memory system with capacity of 64GB. Determine the number of the address lines used in this microcontroller system. *(You are required to show out all working steps)*

[3 marks]

- (d) (i) List out **THREE** shortcomings of using four coupled single-core processors systems as compared to Quad-core processor systems.

[6 marks]

(ii) 80386DX Intel 32-bit microprocessor has six functional units. Name any **TWO** of these functional units and briefly explain their purpose.

[4 marks]

Continued...

Question 2

- (a) Consider available memory ICs are 2Kbytes ROM and 2Kbytes RAM. An 8051 microcontroller system is designed to address 6Kbytes of external data memory followed by 2Kbytes of external program memory.

- (i) Determine the number of ROM ICs and RAM ICs required. [1 Mark]
- (ii) Calculate the size of address bus required. [2 Marks]
- (iii) Show and label the drawing of system configuration showing the 8051 signal lines to be used for data, address and control buses. [10 Marks]

- (b) (i) Determine the byte address and bit position involved in CLR 20 instruction. [2 Marks]
- (ii) Consider the assembly language instruction sequence:

```
MOV A, #168
MOV R1, #0B8H
ADD A, R1
```

Identify the contents of Program Status Word (PSW) and Accumulator (A) after the execution of **EACH** instruction in **binary** format.
(Assume initial value: $A=00H$ and $PSW=00H$)

[5 marks]

Continued...

Question 3

- (a) Consider current content of Program Counter (PC) is 020AH. Determine the minimum and maximum destination address can be supported by each of the following MCS-51 program branching instruction.

LJMP

[2 marks]

- (b) An 8051 subroutine is shown below (assume 12MHz crystal is used):

```

SUB:      MOV R0, #20H
LOOP:    MOV @R0, #0
          INC R0
          CJNE R0, #80H, LOOP
          RET

```

- (i) In how many machine cycles does **each** instruction execute (please answer in the order of instruction of appearance)? [5 marks]
- (ii) How long does this instructions sequence take to execute? [3 marks]
- (iii) How many time the loop execute for this instruction sequence? [2 marks]

- (c) Consider the following MCS-51 assembly language subroutine:

```

ORG 0000H
MOV EFH, #0AH
MOV R6, EFH
MOV A, R6
MOV DPTR, #0EFFH
MOVC A, @A+DPTR
DEC A
END

```

The contents of the on-chip ROM before the execution of the program are shown in Table Q3.

Table Q3

Address	Content
0F08H	02H
0F09H	05H
0F0AH	ABH
0F0BH	CCH

- (i) Determine the content all registers and memory locations affected after the execution of **EACH** instruction. [6 marks]

Continued...

(ii) Determine the size of the program in bytes

[2 marks]

Continued...

Question 4

- (a) Assume that XTAL = 12 MHz, what value do you need to load in to the timer registers if you want to have a delay of 6ms (assume no looping to have delay of 6ms). Write the program for Timer1 to create a pulse width of 6ms on P2.1.

[10 marks]

- (a) Write a program to transmit "Y", "E", and "S" continuously through a serial port at 4800 baud rate, using 8-bit ASCII code, along with one stop bit. Use Timer1 to provide the clock for the required baud rate. (*Assume 11.0592MHz crystal frequency, SMOD = 1*)

[10 marks]

Continued...

Question 5

(a)

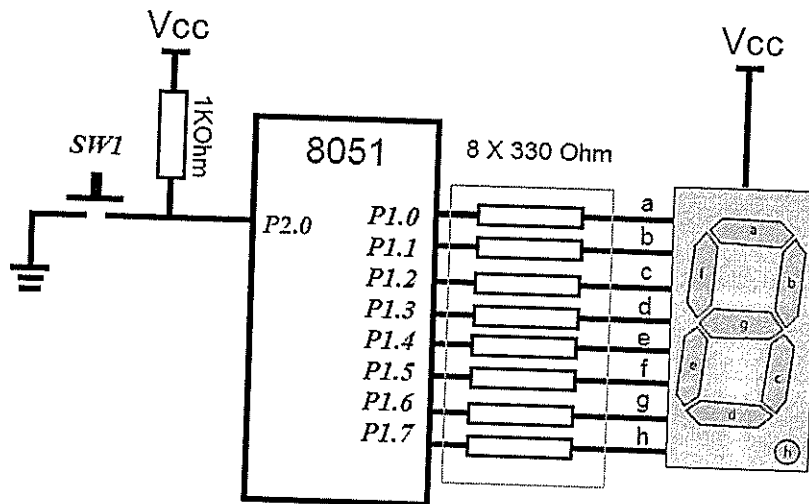


Figure Q5(a)

Figure Q5(a) shows an 8051 microcontroller interfaces to a press button SW1 on port pin 2.0, and a **common anode** seven-segment LED display device on Port 1. Table Q5(a) tabulates the bit patterns for each character to decode the seven-segment LED display.

Table Q5(a)

	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Character	h	g	f	e	d	c	b	a
Y	1	0	0	1	0	0	0	1
E	1	0	0	0	0	1	1	0
S	1	0	0	1	0	0	1	0

Assume 1 second delay subroutine *ONESEC* is available. Write a MCS-51 assembly language program to perform the following tasks:

- Once the SW1 is pressed and hold, seven-segment LED display will repeatedly display the characters in sequence starting from Y, E, and S.
- Time duration for each character to be displayed is 1 second.
- The display will be stopped only if SW1 is released.

[7 marks]

Continued ...

- (b) An 8051 microcontroller based *Automated Vanilla Cake Mixer-Baker System* is shown in Figure Q5(b).

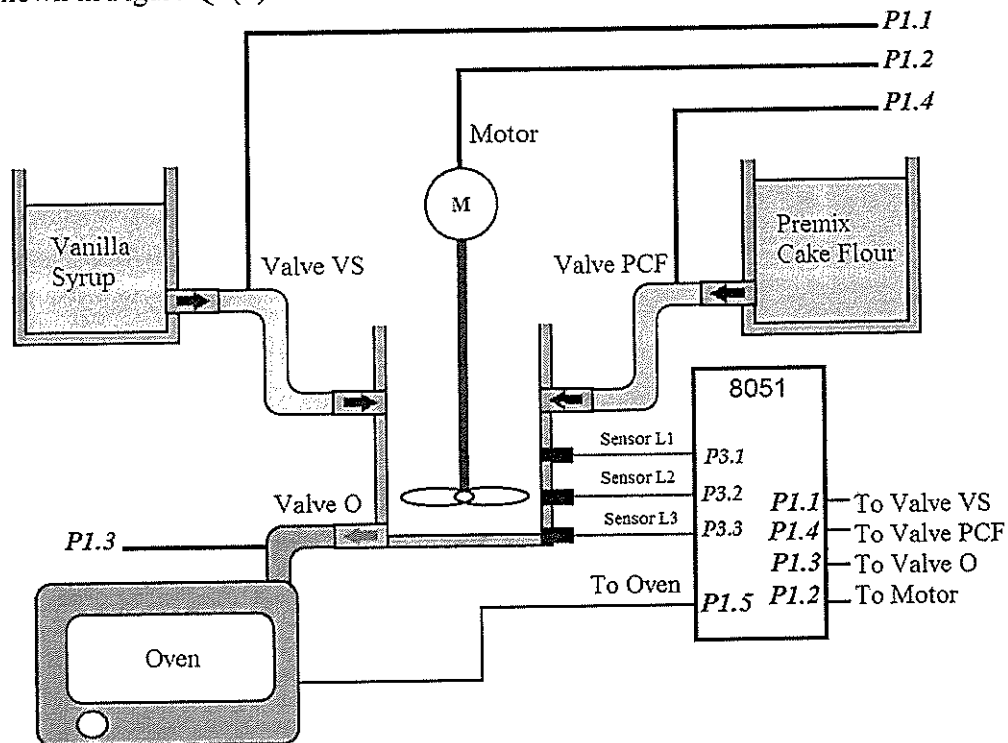


Figure Q5(b)

- The tank has three level sensors that send signals to input lines **P3.1** to **P3.3**. A logical **HIGH** from the sensor indicates that the level has been reached.
- The output lines **P1.1**, **P1.4**, and **P1.3** provide signals to the solenoid valves. A logical **HIGH** from the lines will open the corresponding valve.
- The output lines **P1.2** and **P1.5** provide signals to the stirring motor and oven respectively which are both activated by a logical **HIGH**.

Continued ...

The machine performs the following process sequences:

1. Initially, all valves, oven and motor are closed.
2. The mixer tank is first loaded with vanilla syrup through a solenoid *Valve VS*.
3. When the vanilla syrup reaches level indicated by *Sensor L2*, *Valve VS* is closed and the tank is now loaded with premix cake flour through *Valve PCF*.
4. When the mixture in the tank reaches level indicated by *Sensor L1*, *Valve PCF* is closed.
5. The stirring motor *M* starts the stirring process that last for approximately 1 minute.
6. After that, the dispensing *Valve O* opens to drain the mixture into oven.
7. When the mixture reaches level indicated by *Sensor L3*, *Valve O* is closed
8. Then, *Oven* is turned on for baking process last for approximately 30 minutes.
9. Finally, the whole process is stop.

Write a MCS-51 assembly language program to carry out the process. Assume 12MHz crystal frequency is used.

[13 marks]

End of Page

APPENDIX

Special Function Register Formats

Interrupt Enable (IE)

Bit Addr.	AFH	-	-	ACH	ABH	AAH	A9H	A8H
Name	EA	-	-	ES	ET1	EX1	ET0	EX0

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IE.7	EA	Global enable/disable. EA = 1, each individual source is enabled/disabled by setting/clearing its enable bit. EA = 0, disable all interrupts.
IE.6	-	Undefined
IE.5	-	Not implemented in 8051. ET2 for 8052.
IE.4	ES	Serial port interrupt enable bit.
IE.3	ET1	Timer 1 interrupt enable bit.
IE.2	EX1	External interrupt enable bit.
IE.1	ET0	Timer 0 interrupt enable bit.
IE.0	EX0	External interrupt enable bit.

Interrupt Priority (IP)

Bit Addr.	-	-	-	BCH	BBH	BAH	B9H	B8H
Name	-	-	-	PS	PT1	PX1	PT0	PX0

BIT	SYMBOL	FUNCTION (Enable=1, Disable=0)
IP.7	-	Undefined
IP.6	-	Undefined
IP.5	-	Not implemented in 8051. PT2 for 8052.
IP.4	PS	Serial port interrupt priority bit.
IP.3	PT1	Timer 1 interrupt priority bit.
IP.2	PX1	External interrupt priority bit.
IP.1	PT0	Timer 0 interrupt priority bit.
IP.0	PX0	External interrupt priority bit.

Interrupt Vectors

Interrupt Source	Flag	Vector Address
System Reset	RST	0000H
External 0	IE0	0003H
Timer 0	TF0	000BH
External 1	IE1	0013H
Timer 1	TF1	001BH
Serial Port	RI & TI	0023H
Timer 2 (8052)	TF2 or EXF2	002BH

APPENDIX

Program Status Word (PSW)

Bit Addr.	D7H	D6H	D5H	D4H	D3H	D2H	-	D0H
Name	CY	AC	F0	RS1	RS0	OV	-	P

Serial Control (SCON)

Bit Addr.	9FH	9EH	9DH	9CH	9BH	9AH	99H	98H
Name	SM0	SM1	SM2	REN	TB8	RB8	TI	RI

BIT	SYMBOL	FUNCTION
SCON.7	SM0	Serial port mode bit 0 (see Table A.1).
SCON.6	SM1	Serial port mode bit 1 (see Table A.1).
SCON.5	SM2	Serial port mode bit 2; enables multiprocessor communications in modes 2 and 3; RI will not be activated if received 9 th bit is 0. In mode 1, if SM2 = 1, then RI will be activated only if a valid stop bit was received. In mode 0, SM2 should be 0.
SCON.4	REN	Receiver enable; must be set to receive characters.
SCON.3	TB8	Transmit bit 8; 9 th bit transmitted in modes 2 and 3; set/cleared by software.
SCON.2	RB8	Receive bit 8; 9 th bit received.
SCON.1	TI	Transmit interrupt flag; set at end of character transmission; cleared by software.
SCON.0	RI	Receive interrupt flag; set at end of character reception; cleared by software.

Table A.1 The 8051 Serial Port Mode Selection

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	Fixed
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fixed
1	1	3	9-bit UART	Variable

APPENDIX

Timer Control (TCON)

Bit Addr.	8FH	8EH	8DH	8CH	8BH	8AH	89H	88H
Name	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

BIT	SYMBOL	FUNCTION
TCON.7	TF1	Timer-1 overflow flag. Set by hardware on overflow. Cleared by hardware when processor vectors to interrupt routine. Must be cleared by software when not involve interrupt
TCON.6	TR1	Timer-1 run control bit. Set/cleared by software to turn timer/counter on/off.
TCON.5	TF0	Timer-0 overflow flag. Do the same function as TF1 but for Timer-0.
TCON.4	TR0	Timer-0 run control bit. Do the same function as TR1 but for Timer-0.
TCON.3	IE1	External interrupt-1 edge flag. Set by hardware when interrupt-1 falling edge is detected. Cleared by hardware when interrupt is processed.
TCON.2	IT1	Interrupt-1 Type control bit. Set/cleared by software to specify falling edge/low level triggered external interrupts.
TCON.1	IE0	External interrupt-0 edge flag. Do the same function as IE1 but for external interrupt-0.
TCON.0	IT0	Interrupt-0 Type control bit. Do the same function as IT1 but for external interrupt-0.

Timer Mode (TMOD)

Bit	7	6	5	4	3	2	1	0
Name	GATE	C/T	M1	M0	GATE	C/T	M1	M0

BIT	SYMBOL	FUNCTION
TMOD.7	GATE1	When this bit is set the timer will only run when INT1 (P3.3) is high (hardware control). When this bit is cleared the timer will run regardless of the state of INT1 (software control).
TMOD.6	C/T1	Timer / Counter select bit. $C / \bar{T} = 0 \rightarrow$ Timer operation. $C / \bar{T} = 1 \rightarrow$ Counter operation.
TMOD.5	M1	Mode selection bits (see Table A.2). [for timer 1]
TMOD.4	M0	Mode selection bits (see Table A.2). [for timer 1]
TMOD.3	GATE0	Exactly the same function as GATE1 but for Timer0
TMOD.2	C/T0	Exactly the same function as C/T1 but for Timer0
TMOD.1	M1	Mode selection bits (see Table A.2). [for timer 0]
TMOD.0	M0	Mode selection bits (see Table A.2). [for timer 0]

Table A.2 Timer Mode Selection

M1	M0	Timer Mode	Description of Mode
0	0	0	13-bit Timer
0	1	1	16-bit Timer
1	0	2	8-bit auto-reload
1	1	3	Split timer mode

MCS-51 Opcode Map

byts Instruction operands cycle	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP 1C	JBC bit, rel 2C	JB bit, rel 2C	JNB bit, rel 2C	JC rel 2C	JNC rel 2C	JZ rel 2C	JNZ rel 2C	SJMP rel 2C	MOV DPTR, #data16 2C	ORL C, bit 2C	ANL C, bit 2C	PUSH dir 2C	POP dir 2C	MOVX A, @DPTR 1C	MOVX @DPTR, A 1C
1	AJMP (P0) 2C	ACALL (P0) 2C	AJMP (P1) 2C	ACALL (P1) 2C	AJMP (P2) 2C	ACALL (P2) 2C	AJMP (P3) 2C	ACALL (P3) 2C	AJMP (P4) 2C	ACALL (P4) 2C	AJMP (P5) 2C	ACALL (P5) 2C	AJMP (P6) 2C	ACALL (P6) 2C	AJMP (P7) 2C	ACALL (P7) 2C
2	LJMP addr16 3C	RR A 1C	RRC A 1C	RLC A 1C	ORL dir, A 1C	ANL dir, A 1C	XRL dir, #data 1C	XRL dir, #data 1C	ANL C, bit 2C	ANL C, bit 2C	MOV C, bit 1C	CPL bit 1C	CLR bit 1C	SETB bit 1C	MOVX A, @R0 2C	MOVX @R0, A 2C
3	RR A 1C	RRC A 1C	RL A 1C	RLC A 1C	ORL dir, #data 1C	ANL dir, #data 1C	XRL dir, #data 1C	XRL dir, #data 1C	MOV C, bit 1C	MOV C, bit 1C	MOV C, bit 1C	CPL C 1C	CLR C 1C	SETB C 1C	MOVX A, @R1 2C	MOVX @R1, A 2C
4	INC A 1C	DEC A 1C	ADD A, #data 1C	ADDC A, #data 1C	ORL A, #data 1C	ANL A, #data 1C	XRL A, #data 1C	XRL A, #data 1C	DIV AB 4C	SUBB A, #data 1C	MUL AB 4C	CJNE A, #data, rel 2C	SWAP A 1C	DA A 1C	CLR A 1C	CPL A 1C
5	INC dir 1C	DEC dir 1C	ADD A, dir 1C	ADDC A, dir 1C	ORL A, dir 1C	ANL A, dir 1C	XRL A, dir 1C	XRL A, dir 1C	MOV dir, dir 1C	SUBB A, dir 1C	MOV dir, dir 1C	CJNE A, dir, rel 2C	XCH A, dir 1C	DJNZ dir, rel 2C	MOV A, dir 1C	MOV dir, A 1C
6	INC @R0 1C	DEC @R0 1C	ADD A, @R0 1C	ADDC A, @R0 1C	ORL A, @R0 1C	ANL A, @R0 1C	XRL A, @R0 1C	XRL A, @R0 1C	MOV dir, @R0 1C	SUBB A, @R0 1C	MOV dir, @R0 1C	CJNE @R0, #data, rel 2C	XCH A, @R0 1C	XCHD A, @R0 1C	MOV A, @R0 1C	MOV @R0, A 1C
7	INC @R1 1C	DEC @R1 1C	ADD A, @R1 1C	ADDC A, @R1 1C	ORL A, @R1 1C	ANL A, @R1 1C	XRL A, @R1 1C	XRL A, @R1 1C	MOV dir, @R1 1C	SUBB A, @R1 1C	MOV dir, @R1 1C	CJNE @R1, #data, rel 2C	XCH A, @R1 1C	XCHD A, @R1 1C	MOV A, @R1 1C	MOV @R1, A 1C
8	INC R0 1C	DEC R0 1C	ADD A, R0 1C	ADDC A, R0 1C	ORL A, R0 1C	ANL A, R0 1C	XRL A, R0 1C	XRL A, R0 1C	MOV dir, R0 1C	SUBB A, R0 1C	MOV dir, R0 1C	CJNE R0, #data, rel 2C	XCH A, R0 1C	DJNZ R0, rel 2C	MOV R0, A 1C	MOV A, R0 1C
9	INC R1 1C	DEC R1 1C	ADD A, R1 1C	ADDC A, R1 1C	ORL A, R1 1C	ANL A, R1 1C	XRL A, R1 1C	XRL A, R1 1C	MOV dir, R1 1C	SUBB A, R1 1C	MOV dir, R1 1C	CJNE R1, #data, rel 2C	XCH A, R1 1C	DJNZ R1, rel 2C	MOV R1, A 1C	MOV A, R1 1C
A	INC R2 1C	DEC R2 1C	ADD A, R2 1C	ADDC A, R2 1C	ORL A, R2 1C	ANL A, R2 1C	XRL A, R2 1C	XRL A, R2 1C	MOV dir, R2 1C	SUBB A, R2 1C	MOV dir, R2 1C	CJNE R2, #data, rel 2C	XCH A, R2 1C	DJNZ R2, rel 2C	MOV R2, A 1C	MOV A, R2 1C
B	INC R3 1C	DEC R3 1C	ADD A, R3 1C	ADDC A, R3 1C	ORL A, R3 1C	ANL A, R3 1C	XRL A, R3 1C	XRL A, R3 1C	MOV dir, R3 1C	SUBB A, R3 1C	MOV dir, R3 1C	CJNE R3, #data, rel 2C	XCH A, R3 1C	DJNZ R3, rel 2C	MOV R3, A 1C	MOV A, R3 1C
C	INC R4 1C	DEC R4 1C	ADD A, R4 1C	ADDC A, R4 1C	ORL A, R4 1C	ANL A, R4 1C	XRL A, R4 1C	XRL A, R4 1C	MOV dir, R4 1C	SUBB A, R4 1C	MOV dir, R4 1C	CJNE R4, #data, rel 2C	XCH A, R4 1C	DJNZ R4, rel 2C	MOV R4, A 1C	MOV A, R4 1C
D	INC R5 1C	DEC R5 1C	ADD A, R5 1C	ADDC A, R5 1C	ORL A, R5 1C	ANL A, R5 1C	XRL A, R5 1C	XRL A, R5 1C	MOV dir, R5 1C	SUBB A, R5 1C	MOV dir, R5 1C	CJNE R5, #data, rel 2C	XCH A, R5 1C	DJNZ R5, rel 2C	MOV R5, A 1C	MOV A, R5 1C
E	INC R6 1C	DEC R6 1C	ADD A, R6 1C	ADDC A, R6 1C	ORL A, R6 1C	ANL A, R6 1C	XRL A, R6 1C	XRL A, R6 1C	MOV dir, R6 1C	SUBB A, R6 1C	MOV dir, R6 1C	CJNE R6, #data, rel 2C	XCH A, R6 1C	DJNZ R6, rel 2C	MOV R6, A 1C	MOV A, R6 1C
F	INC R7 1C	DEC R7 1C	ADD A, R7 1C	ADDC A, R7 1C	ORL A, R7 1C	ANL A, R7 1C	XRL A, R7 1C	XRL A, R7 1C	MOV dir, R7 1C	SUBB A, R7 1C	MOV dir, R7 1C	CJNE R7, #data, rel 2C	XCH A, R7 1C	DJNZ R7, rel 2C	MOV R7, A 1C	MOV A, R7 1C